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| Serial No: |
| **2nd Midterm Exam** |
| **Total Time:1 Hour** |
| **Total Marks: 50** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227 Digital**  **Logic Design** |
| Monday 27th March, 2017 |
| **Course Instructor** |
| Dr Mehwish Hasan, Ms Mehreen Alam & Mr. Jawad Hassan |

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## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

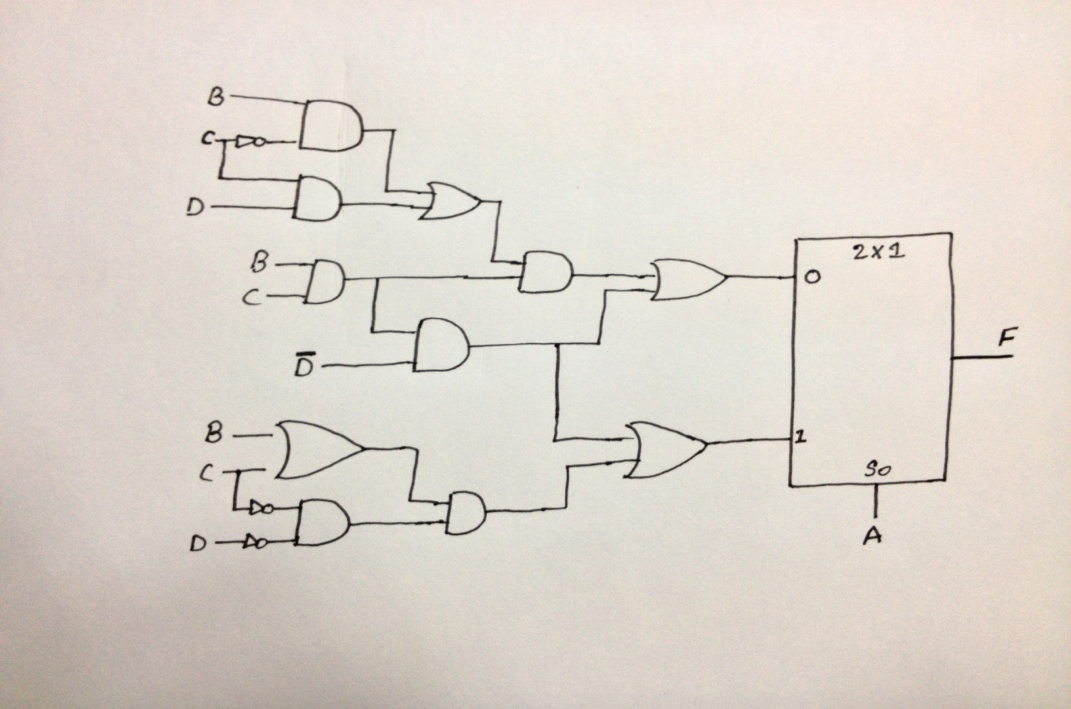
1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use and mark the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **Nine (9)** different printed pages including this Title page and a rough work page at the end. There are total of **five 5** questions.
5. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
6. For each question show your complete method in solution.

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|  | Q-1 | Q-2 | Q-3 | Q-4 | Q-5 | Total |
| **Total**  **Marks** | 5 | 10 | 10 | 18 | 7 | **50** |
| **Marks Obtained** |  |  |  |  |  |  |

**Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Q1. [ 5 pts] Design a half-adder (inputs: A, B, outputs: S and Cout) using only 2-input NOR gates. For full credit, you must use minimum number of gates as possible.**

**Q2. [ 10 pts] What function is implemented by the following 2 x 1 MUX implementation? Do show intermediary output functions for full credit.**



**Q3. [ 2+4+4+2 = 10 pts] Consider a 4-bit priority encoder with the priority sequence D1 > D0 > D3 > D2.**

**a. Write the priority table.**

**b. Write the complete 4-bit table.**

**c. Write minimized equations.**

**d. Draw the resultant circuit diagram. Do not show the internal encoder implementation.**

**Question No.4 [2 + 4 + 6 + 6 = 18]**

**Q4. [ 2+4+6+6 = 18] Design a combinational circuit for data integrity (data correctness using parity bit) checker that has four inputs A3, A2, A1, and A0 and one output Fi. The output will used to implement odd parity i.e., the output Fi = 1 when input has even number of 1's and 0 otherwise.**

**a. Construct truth table for Fi**

**b. Minimize the function and draw the circuit**

**c. Implement the function Fi using 3 x 8 decoders with enable lines.**

**d. Implement the function Fi using 2 x 4 decoders with enable lines.**

**Q5. [ 3+4 = 7 pts] Draw SR latch with NAND gate and give its function table.**

**ROUGH WORK SHEET**